Altera ISP-Based CPLDs & Concurrent Programming

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In a high-volume printed circuit board (PCB) manufacturing environment, time is critical for designers facing time-to-market demands. For this reason, Altera offers designers and manufacturing engineers programming options that minimize production time and increase throughput. One of these options is concurrent programming, which is the simultaneous programming of multiple complex programmable logic devices (CPLDs) that support in-system programmability (ISP). This technical brief compares concurrent programming to traditional CPLD programming (i.e., sequential programming), and discusses concurrent programming through the Joint Test Action Group (JTAG) interface for Altera® MAX® 9000 and MAX 7000S devices.

Concurrent Programming vs. Sequential Programming

For a board with multiple ISP-based CPLDs, you can use concurrent programming to decrease in-system programming time. This programming time is slightly longer than the time needed to program the largest device on the board. In contrast, traditional CPLD programming requires devices to be programmed sequentially (i.e., one device at a time); programming time is equal to the sum of the individual programming times for all CPLD devices. Even if only a few CPLDs on a PCB need to be programmed, sequential programming requires more time to program all the devices on a board than concurrent programming.

Table 1 compares concurrent programming and sequential programming times, using a PCB with 18 devices. With sequential programming, the PCB takes 65 seconds longer to program than with concurrent programming. In a high-volume manufacturing environment, where thousands of boards may need to be programmed and tested, concurrent programming can substantially reduce the time needed to bring a product to market.

Table 1. Example Comparison of Concurrent Programming vs. Sequential Programming

Programming	Devices per Board	Programming Time per Device (seconds)	Total Programming Time (seconds)
Sequential programming	18	4	72
Concurrent programming	18	4	7

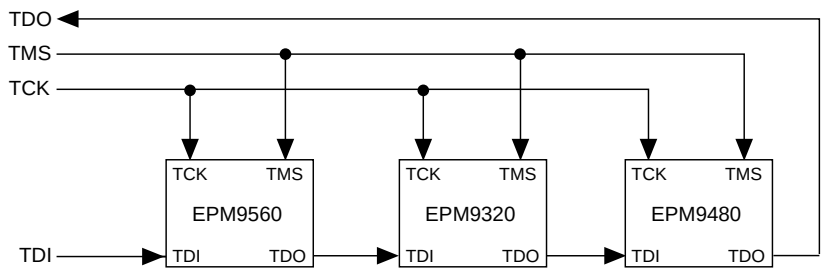
Programming through JTAG

Concurrent programming of ISP-based CPLDs through the JTAG interface reduces the complexity of the manufacturing process. During production, implementing ISP through the JTAG interface allows all the ISP-based devices to be chained together in a JTAG chain, simplifying programming and testing. The JTAG chain can be extended to include non-ISP-based JTAG devices for easier device testing. The programming time for the JTAG chain is slightly longer than the time needed to program the largest device in the chain.

Concurrent Programming in Altera ISP-Based CPLDs

Although devices in a JTAG chain can be programmed sequentially, Altera ISP-based CPLDs allow devices within the same device family to be programmed concurrently, which reduces programming times. This capability allows a chain of MAX 9000 or MAX 7000S devices to be simultaneously programmed. During concurrent programming, data is serially shifted into multiple devices along the JTAG chain, then programming pulses are applied simultaneously to all the devices. Figure 1 illustrates the use of concurrent programming of three Altera MAX 9000 devices through a JTAG chain.

Figure 1. Concurrent Programming Through a JTAG Chain of Three MAX 9000 Devices



The time required to concurrently program multiple devices in a JTAG chain can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \sum_{\text{All Devices}} \frac{Cycle_{PTCK}}{F_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells for only the largest device
$Cycle_{PTCK}$ = Number of TCK cycles to program each device
f_{TCK} = TCK frequency

Table 2 shows the concurrent programming times for 1, 2, 10, and 100 devices in a JTAG chain.

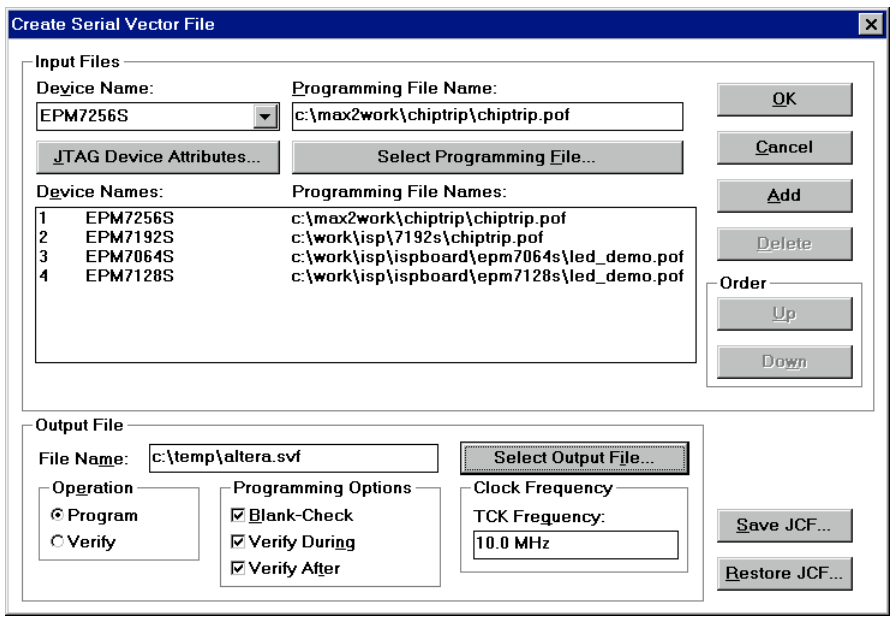
Table 2. Concurrent Programming Times

Family	Device	Programming Times (Seconds) *Note (1)*			
		1 Device	2 Devices	10 Devices	100 Devices
MAX 9000	EPM9560	4.82	5.24	8.57	46.04
	EPM9480	4.71	5.08	8.10	41.98
	EPM9400	4.60	4.93	7.63	37.91
	EPM9320	4.49	4.78	7.16	33.85
MAX 7000S	EPM7256S	2.41	2.57	3.86	18.37
	EPM7192S	2.13	2.25	3.21	14.01
	EPM7160S	1.99	2.09	2.90	11.98
	EPM7128S	1.89	1.97	2.65	10.20
	EPM7096S	1.75	1.82	2.35	8.35
	EPM7064S	1.65	1.71	2.11	6.71
	EPM7032S	1.48	1.51	1.79	4.93

Note:
(1) Times are provided for devices programmed at 10 MHz.

To perform concurrent programming in Altera devices, the Serial Vector Format File (**.svf**) for each device must be merged into a single file, allowing the automated test equipment (ATE) or embedded processor to correctly shift in the data and perform the concurrent programming. Altera ISP users will benefit from this process on the manufacturing floor, because concurrently programming a device with ATE decreases the programming time, thereby decreasing the production time. Figure 2 shows the **Create Serial Vector File** dialog box as it appears in the Altera MAX+PLUS® II software.

Figure 2. Create Serial Vector File Dialog Box



The documents listed below provide more detailed information. Part numbers are in parentheses.

- *Application Note 39: JTAG Boundary-Scan Testing in Altera Devices (A-AN-039-03)*
- *Application Note 85: In-System Programming Times for MAX 9000 & MAX 7000S Devices (A-AN-085-01)*

You can request documents from:

- Altera Literature Services at (888) 3-ALTERA
- Altera Express fax services at (800) 5-ALTERA
- World-wide web at **http://www.altera.com**